



CAD Design Software  
303 Twin Dolphin Drive, Suite 600, Redwood City, CA 94065, USA

## 2014- 2021 - Release Notes Version 8.2.xxx

### Electronics Packaging Designer v8.2 Release Notes:

#### **AutoCAD**

AutoCAD 2007 (17.0)  
AutoCAD 2008 (17.1)  
AutoCAD 2009 (17.2)  
AutoCAD 2010 (18.0)  
AutoCAD 2011 (18.1)  
AutoCAD 2012 (18.2)  
AutoCAD 2013 (19.0)  
AutoCAD 2014 (19.1)  
AutoCAD 2015 (20.0)  
AutoCAD 2016 (20.1)  
AutoCAD 2017 (21.0)  
AutoCAD 2018 (22.0)  
AutoCAD 2019 (23.0)  
AutoCAD 2020 (23.1)

#### **BricsCAD**

BricsCAD v14.2  
(increments 14.2.16+)  
BricsCAD v15.1  
(increments 15.1.04+)  
BricsCAD v16.2  
(increments 16.2.09+)  
BricsCAD v17.2  
(increments 17.2.06-1+)  
BricsCAD v18.1  
(increments 18.1.09+)  
BricsCAD v19.1  
(increments 19.10.10+)

#### **EPD 8.1 OEM**

**No longer sold or supported**



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## General Updates:

- Licensing system and Vendor Daemon updated to FlexNET v11.12
- Improved 3D Bondwire clearance checking technology works on 3D EPD-created JEDEC wires.
- MS Excel netlist import using BGANETWIZ now combines cells containing multiple numbers in parenthesis and applies to multiple pin in drawing. Works best on power nets containing multiple pins for one signal net.

## IC Packaging

- Supports Jedec-4 and Jedec-5 bondwire profiles wherever profiles are used
- LFINTEL has improved algorithm for calculation of via when exporting downsets to 3<sup>rd</sup>-party applications
- LFINTEL stores original entities for easy rerun of intelligization
- LFINTEL supports user-drawn substrate bondpads
- LFINTEL ability to draw centerline on the leadtips
- ATTACH supports a new fanout type (staggered multi-row straight aligned)
- PLACEDIE supports Ribbon bondwires
- PLACEDIE supports copper bondwires
- DIEMAKE supports user-drawn component bondpads with irregular shapes
- ATTINTEL supports down-bonds

## Netlist Capture

- Accurately capture irregular shape component bondpads
- Captures “clips” in leadframes
- Captures “heatslugs” in leadframes

## MakeEdge

- Completely new region modeler operates on true arcs.
- New capabilities for processing of holes (voids) in the result



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## **Bondwire Export**

- Exports XML format to HK bonding machines

## **Auto Schematic Capture**

- Library components may contain arcs in polylines
- Ability to cancel if the schematic environment is accidentally loaded
- Un-connect marks are not corrupted during drawing save

## **Printed Resistors**

- Supports a third pin on the TOPHAT configuration

## **Design Rule Checking**

- ADRC now supports Line entities
- ADRC supports filtering at the rule-group level
- ADRC includes new Rule #175 for 3D bondwire clearance checking (available as a separate license).

## **Import/Export**

- GDSOUT ability to convert true type text to polygons

## **3D PCB**

- Improved 3D down-set slopes compatibility with Ansys and Cadence



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## 3<sup>rd</sup> Party Links Export:

- Added Support for new versions of Ansys and CST Microwave Studio
- Added new function to use EPD-Created JEDEC wire profiles.

## New Commands

- **EPDEXTRUDE** – An EPD-compatible Extrude command to use as an alternative to the native Extrude command.
- **JEDECPROFILE** parametrically creates JEDEC 4 & 5 bondwire profiles for use with EPD 3D commands, Bondwire Clearance checking and Export to Ansys.